at least one of the stored instruction in an event of a downstream stall on the selected one of the plurality of threads.

37. (New) The microprocessor according to claim 36, wherein the at least one upstream pipeline unit includes at least one of a trace cache and a micro-instruction sequencer.

38. (New) The microprocessor according to claim 36, wherein the downstream pipeline unit includes an execution unit.

39. (New) The microprocessor according to claim 36, wherein the instruction queue is configured to select one of the threads based on available resources.

40. (New) The microprocessor according to claim 36, wherein the instruction queue is configured to alternate between the plurality of threads when passing the instructions.

41. (New) The microprocessor according to claim 36, wherein the instruction queue is configured to pass instructions on one of the threads, and configured to switch to a different one of the threads when a stall is detected on the one of the threads.

42. (New) The microprocessor according to claim 36, wherein the instruction queue includes:

a memory device to store the instructions; and

an output multiplexer which is configured, in a first mode of operation, to pass instructions from the upstream pipeline unit to the downstream pipeline unit, and which is configured, in a second mode of operation, to reissue the at least one of the stored instructions.

Remarks

Applicants have canceled claims 1-27, without prejudice, and have added new claims 28-42. The Specification has been amended to identify the parent application and to incorporated the parent application by reference.

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It is respectfully submitted that the present invention is new, non-obvious and useful. Prompt consideration and allowance is therefore respectfully requested.

Respectfully submitted,

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